CLAIMS

1. A semiconductor device having a semiconductor body (22) comprising an active area (7) and a termination structure (16) surrounding the active area, the termination structure comprising a plurality of lateral transistor devices (2a to 2d) connected in series and extending from the active area towards a peripheral edge (42) of the semiconductor body, with a zener diode (8) connected to the gate electrode (4) of one of the lateral devices for controlling its gate voltage, such that a voltage difference between the active area and the peripheral edge is distributed across the lateral devices and the zener diode.

2. A semiconductor device of Claim 1 wherein a zener diode (8) is connected between each pair of adjacent lateral transistors (2a to 2d).

3. A semiconductor device of Claim 2 wherein each zener diode (8) is connected between the source electrode (10) of the lateral transistor of the corresponding pair closer to the active area (7) and the gate electrode (4) of the other lateral transistor of the corresponding pair.

4. A semiconductor device of Claim 2 wherein each zener diode (8) is connected between the gate electrodes (4) of the corresponding pair of lateral transistors.

5. A semiconductor device of any preceding Claim wherein each lateral device (2a to 2d) comprises a gate electrode (31) insulated from the semiconductor body (22) by a layer (32) of gate insulating material, the gate electrodes and layers of gate insulating material of the lateral devices being formed in the same respective process steps as insulated electrodes (11) and layers (25) of material insulating the insulated electrodes of devices in the active area (7).

6. A semiconductor device of Claim 5 wherein the active area (7) comprises trench-gate semiconductor devices and the lateral transistors of the termination structure (16) are trench-gate transistors.

7. A semiconductor device of Claim 5 or Claim 6 wherein each lateral device (2a to 2d) comprises a trench (30) having the gate electrode (31) therein, the trenches of the lateral devices being formed in the same respective process steps as gate trenches (20) of devices in the active area (7).

8. A semiconductor device of Claim 5 wherein the active area (7) comprises planar gate semiconductor devices and the lateral transistors of the termination structure (16) are planar gate transistors.

9. A semiconductor device of any preceding Claim wherein the lateral devices (2a to 2d) include a region (15) of a first conductivity type over an underlying region (14a) of a second, opposite conductivity type, and wherein the active area (7) comprises devices having a region (15) of the first conductivity type which is formed in the same process step as the first conductivity type region of the lateral devices.

10. A semiconductor device of any preceding Claim wherein the gate electrodes (31) of the lateral devices are formed of polycrystalline silicon, and the zener diode (8) is formed of polycrystalline silicon deposited in the same process step as the gate electrodes.

11. A method of forming a semiconductor device having a semiconductor body (22) comprising an active area (7) and a termination structure (16) surrounding the active area, the termination structure comprising a plurality of lateral transistor devices (2a to 2d) connected in series and extending from the active area towards a peripheral edge (42) of the semiconductor body, with a zener diode (8) connected to the gate electrode

(4) of one of the lateral devices for controlling its gate voltage, such that a voltage difference between the active area and the peripheral edge is distributed across the lateral devices and the zener diode, wherein the gate electrodes (31) of the lateral devices are formed of polycrystalline silicon, and the method comprises forming the zener diode (8) of polycrystalline silicon deposited in the same process step as the gate electrodes.

12. A method of Claim 11 wherein each lateral device (2a to 2d) comprises a trench (30) having the gate electrode (31) therein, and the method comprises forming the trenches of the lateral devices in the same respective process steps as gate trenches (20) of devices in the active area (7).

13. A semiconductor device substantially as described herein with reference to the accompanying Drawings.

14. A method of forming a semiconductor device substantially as described herein with reference to the accompanying Drawings.